REMARKS

Status of Claims:

New claims 14-20 are added. Thus, claims 1-20 are present for examination.

Specification:

The abstract of the disclosure is objected to because it appears to exceed the 150-word limit. (MPEP 608.01(b)).

The abstract of the disclosure has been amended and has less than 150 words. Therefore, the abstract is now believed to be in compliance with the requirements of MPEP 608.01(b).

The specification has been further amended to correct a minor informality.

Claim Rejection Under 35 U.S.C. 112:

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, as amended, the rejection is respectfully traversed.

The Examiner states that, "[c]laim 1 recites the limitation 'information' ", and that, "[t]here is insufficient antecedent basis for this limitation in the claim."

Independent claim 1 has been amended to remove "the" before "information" and, thus, independent claim 1, as amended, is believed to be in compliance with the requirements of 35 U.S.C. 112, second paragraph.

Claim Rejections Under 35 U.S.C. 103:

Claims 1-5 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hariguchi (U.S. Patent No. 6,181,698) in view of Nakamura et al. (U.S. Patent No.

6,553,031) (hereinafter Nakamura) and further in view of Hayashi (U.S. Patent No. 6,741,596).

Claims 6 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hariguchi in view of Nakamura, further in view of Hayashi, and further in view of Takase et al. (U.S. Patent No. 6,411,620) (hereinafter Takase).

With respect to claims 1-13, as amended, the rejections are respectfully traversed.

Independent claim 1, as amended, recites a packet processing unit, comprising:

"packet receiving means for outputting a packet received via a first transmission channel in the form of **split cells of a fixed length**,

search key extracting means for extracting a predetermined search key from said cells output from said packet receiving means,

a CAM for performing retrieval of a memory address based on said search key extracted by said search key extracting means and for outputting said memory address,

associative data storing means for storing at least destination information and for outputting information stored at an input memory address,

associative data reading means for calculating a particular memory address of said associative data storing means based on said memory address output from said CAM and for supplying the particular memory address to said associative data storing means,

destination address means for updating a destination address of a particular cell of said cells based on particular information output from said associative data storing means that is stored at said particular memory address in said associative data storing means and for outputting said cells, and

packet transmitting means for **combining the cells** output from said destination address means into an updated packet and for outputting said updated packet to a second transmission channel,

wherein said packet receiving means, said search key extracting means, said CAM, said associative data reading means, said associative data storing means, said destination address means, and said packet transmitting means are configured to perform processing as **stages of a pipeline**." (Emphasis Added).

A packet processing unit including the above-quoted features has at least the advantages that: (i) a packet receiving means outputs a packet received via a first transmission channel in the form of **split cells of a fixed length**; (ii) a search key extracting means extracts a predetermined search key from the cells output from the packet receiving means; (iii) a CAM performs retrieval of a memory address based on the search key extracted by the search key extracting means and outputs the memory address; and (iv) the packet receiving means, the search key extracting means, the CAM, an associative data reading means, an associative data storing means, a destination address means, and a packet transmitting means are configured to perform processing as **stages of a pipeline**. (Specification; page 2, line 14 to page 3, line 17; page 7, line 15 to page 10, line 2; page 11, line 3 to page 13, line 28; abstract; Figs. 1-2).

Neither Hariguchi, Nakamura, nor Hayashi, alone or in combination, disclose or suggest a packet processing unit including the above-quoted features. The Examiner points to figure 3, reference **90** of Hariguchi as disclosing a packet receiving means for outputting the packet received via said transmission channel in the form of cells of a fixed length. (Office Action; page 3). The Examiner then states that, "Hariguchi **does not disclose** splitting a variable length packet into fixed length cells". (Office Action; page 4) (Emphasis Added).

The Examiner then points to Nakamura as disclosing, "splitting variable length packets into fixed length cells in column 4 lines 60-63." (Office Action; page 4). The Examiner then asserts that, "[i]t would have been obvious to one of ordinary skill in the art to include Nakamura's packet split/reassemble procedure in Hariguchi's cell processing unit because doing so conserves circuitry as taught by Nakamura in **column 6 lines 62-64**." (Office Action; page 4) (Emphasis Added). The Examiner states that, "[i]f a variable length packet were to be allowed the bit width would need to be much larger, which would require more input lines." (Office Action; page 4). Finally, the Examiner points to figure 3, reference **94** of Hariguchi as disclosing a search key extracting means for extracting a predetermined search key from said cells received from said packet receiving means. (Office Action; page 3) (Emphasis Added).

However, even if the communication node interface of Nakamura were combined with the router of Hariguchi, the combined system would still not include a packet receiving means for outputting a packet received via a first transmission channel in the form of split cells of a fixed length and a search key extracting means for extracting a predetermined search key **from the cells output from the packet receiving means**. This is due to at least the following three reasons.

First, it is important to understand that figure 3, reference 90 of Hariguchi is not a packet receiving means and does not receive a packet. Instead, figure 3, reference 90 of Hariguchi illustrates an entry address bus 90 that is used to specify a CAM entry 230 during a time of "**configuration**" when the CAM entries 230 are being written with IP addresses and IP prefixes. (Hariguchi; Fig. 3; column 10, lines 13-27). Thus, the entry address bus 90 in the system of Hariguchi is merely used to specify CAM entries to be written to in order to **configure** a CAM before searches are performed. When the configuration/search line 120 of the system of Hariguchi is set to "**configuration**", the word line driver 92 outputs "1" to the word line 70 of the CAM entry 230 specified with the entry address bus 90. (Hariguchi; Fig. 3; column 10, lines 12-18). This allows for an IP address and a corresponding IP prefix to be written into the CAM entry 230 specified with the entry address. (Hariguchi; column 10, lines 16-19).

In the system of Hariguchi, once the configuration/search line 120 is set to "**search**" to search for a route, the word line driver 92 outputs **"0"** onto **all** of the word lines 70. (Hariguchi; Fig. 3; column 10, lines 28-32). As a consequence, any data on the entry address bus 90 during a time of searching in the system of Hariguchi is **irrelevant**, because the word line driver 92 will output **"0"** onto **all** of the word lines 70 when the configuration/search line 120 is set to "**search**" to search for a route. (Hariguchi; Fig. 3; column 10, lines 28-32). Thus, the entry address bus 90 in the system of Hariguchi does not receive a **packet**, but only is used to specify CAM entries during a time of **configuration** when data is written to the CAM entries. Also, the entry address bus 90 in the system of Hariguchi is not even used during a time of **searching** when searching for a route. Therefore, the entry address bus 90 of the system of Hariguchi does not disclose a packet receiving means of the present claim.

Second, the search key input/output lines 94 in the system of Hariguchi do not receive data from the entry address bus 90. (Hariguchi; Fig. 3). Also, the entry address bus 90 in the system of Hariguchi is only used to specify a CAM entry for **configuration**, so it would be useless to extract a **search key** from the data on entry address bus 90, because the data on entry address bus 90 is not used when searching for a route. (Hariguchi; column 10, lines 28-33). In contrast, a packet processing unit of the present claim recites the feature of, "search key extracting means for extracting a predetermined search key from said cells output from said packet receiving means". (Emphasis Added).

Third, the system of Nakamura is configured to determine an output port number for an IP packet from the sub routing table 15 **before** the cell assembler circuit 13 converts the packet into fixed length short packets. (Nakamura; Fig. 5; column 7, lines 37-50). In the system of Nakamura, the sub routing table 15 is a table for temporarily storing copies of some routing information entries held in the main routing table 15. (Nakamura; Figs. 1 and 5; column 7, lines 1-4). The routing table access circuit 14 in the system of Nakamura extracts a destination IP address from a header of each IP **packet** and accesses the sub routing table 15 based on the destination IP address to read out a next hop address 152 and an output port number 153 corresponding to the destination IP address. (Nakamura; column 7, lines 15-25).

Then, in the system of Nakamura, the cell assembler circuit 13 is supplied with a next hop address 152 and an output port number 153 read out from the sub routing table 15, and the cell assembler circuit 13 generates an internal header 71 including the output port number 153 and converts the IP packet to a plurality of fixed length cells. (Nakamura; column 7, lines 37-50). Thus, in the system of Nakamura, a destination IP address is extracted from a **packet** **before** the packet is split into cells. Indeed, in the system of Nakamura, the destination IP address is used to obtain an output port number from a routing table **before** the packet is split into cells by the cell assembler circuit 13.

In contrast, a packet processing unit including the above quoted features allows for a packet to be split into cells, and then for a search key to be extracted from the cells **after** the packet has been split into cells. Therefore, even if the cell assembler circuit 13 of the system of Nakamura were included in the router of Hariguchi, the combined system would search for

a routing result based on a destination IP address extracted from a **packet before** splitting the packet into cells, which is different than a packet processing unit of the present claim that allows for searching for information based on a search key extracted from a **cell after** splitting a packet into cells.

Moreover, there is no motivation in the Hariguchi and Nakamura references to combine the system of Nakamura with the system of Hariguchi. The Examiner points to **column 6, lines 62-64** of Nakamura as providing motivation to include Nakamura's packet split/reassemble procedure into Hariguchi's system. (Office Action; page 4). However, it is important to understand that column 6, lines 62-64 of Nakamura is describing a portion of a line interface board of Nakamura that occurs before the cell assembler circuit 13 splits a packet into cells. Indeed, the cited portion of Nakamura describes the delivery of an IP packet from the input line interface 11 on output signal line L11. (Nakamura; Fig. 5; column 6, lines 62-64). As illustrated in figure 5 of Nakamura, the input line interface 11 and the output signal line L11 are positioned in the line interface board before the cell assembler circuit 13. (Nakamura; Fig. 5). Thus, the splitting of a packet into cells by the cell assembler circuit 13 in the system of Nakamura **has no affect on the bit width of the output signal line L11**, because the splitting of the packet into cells does not occur until after the packet has already been delivered on output signal line L11. (Nakamura; Fig. 5). As a consequence, there would be no motivation to combine the system of Nakamura with the system of Hariguchi.

It is further noted that Hayashi does not cure the deficiencies with respect to the teachings of Hariguchi and Nakamura discussed above. Therefore, independent claim 1, as amended, is neither disclosed nor suggested by the Hariguchi, Nakamura, and Hayashi references and, hence, is believed to be allowable. The Patent Office has not made out a *prima facie* case of obviousness under 35 U.S.C. 103.

The dependent claims are deemed allowable for at least the same reasons indicated above with regard to the independent claim from which they depend. It is noted that, with regard to dependent claims 6 and 10-13, Takase does not cure the deficiencies with respect to the teachings of Hariguchi, Nakamura, and Hayashi discussed above.

New claims 14-20 recite features that are not found in any of Hariguchi, Nakamura, Hayashi, or Takase.

Conclusion:

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date February 22, 2006

By Just Sobaje

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (310) 975-7965
Facsimile: (310) 557-8475

Justin M. Sobaje
Attorney for Applicant
Registration No. 56,252